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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,106	08/14/2001	Stephen E. Jones	149148001US1	9880
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PERKINS COIE LLP			MOLL, JESSE R	
PATENT-SEA				
P.O. BOX 1247			ART UNIT	PAPER NUMBER
SEATTLE, WA 98111-1247			2181	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/930,106	Applicant(s) JONES, STEPHEN E.	
	Examiner Jesse R. Moll	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 03 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3 July 2006 has been entered.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 26-29, 31-32, 35-39, 41-42, 45, 47-50, 52-53 and 56 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. Applicant's specification when filed contains no information pertaining to receiving a signal on a package pin of the processor, receiving a message via an APIC bus or front side bus, receiving the SMI from a Northbridge or Southbridge controller, or indicating a cause that triggered the SMI.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-17 and 26-45 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "an SMI" in line 4. It is unclear whether the limitation refers to the previously mentioned limitation in lines 2-3. Examiner suggests the limitation read "the SMI".

Similar problems exist in claim 5.

All remaining claims are rejected due to their dependence on indefinite parent Claims 1 and 5.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

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applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 18-25, 46 and 54-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Wooten (U.S. Patent No. 5,832, 299) herein referred to as Wooten'299.

6. Referring to claim 18, Wooten'299 discloses, as claimed, a computer-readable medium containing instructions for an SMI routine that allows execution of code that resides in physical address space above address 0x100000, by a method comprising: saving state (such as EIP, and EFLAGS, see Col. 15, lines 36-41, or Col. 16, lines 38-42) of the processor; switching the processor to protected mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E); and before returning from the interrupt, executing code that resides in physical address space above address 0x100000 (this is the existing feature when the Wooten'299's system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30)); code is certainly executed above 0x100000 in a 4GB address space; see col. 11, lines 1-5).

7. As to claim 19, Wooten'299 also discloses: after executing the code, restoring the saved state of the processor and returning from the SMI (the saved state must be restored if the mode is transparent to the other code; see col. 5, lines 55-60).

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8. As to claim 20, Wooten'299 also discloses the code is executed using a global descriptor table that is different from the global descriptor table in use when the SMI occurred (see col. 11, lines 21-38).

9. As to claim 21, Wooten'299 also discloses: the computer system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30).

10. As to claim 22, Wooten'299 also discloses: the method of claim 5 wherein the executing executes 32-bit (note the Wooten'299's protected mode is a flat 32 bit model).

11. As to claim 23, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the instructions are loaded into system management memory (inside such as memory unit 102, see Fig. 1a) by a BIOS.

12. As to claim 24, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the code is loaded into memory from a ROM (110 see Fig. 1A).

13. As to claim 25, Wooten'299 also discloses: the computer-readable medium of claim 18 wherein the code is loaded into memory from a flash ROM (110 see Fig. 1A, note the ROM can be a flash type).

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14. As to claim 46, Wooten'299 also discloses the method is performed in response to the receipt of an SMI by a processor (Virtual System Mode Interrupt, see Col. 15, lines 60-61. Note the Wooten'299's Virtual System Mode is best reasonably and broadly interpreted as the claimed System Management Mode).

15. As to claim 54, Wooten'299 also discloses an electronic circuit is the source of the SMI (an interrupt is generated by a circuit).

16. As to claim 55, Wooten'299 also discloses returning from the interrupt by executing an RSM instruction (any means for returning from the SMI could be considered a return from system mode instruction).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claims 1-17, 33, 34, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of Russell et al. (U.S. Patent No. 6,751,737) herein referred to as Russell.

19. Referring to claim 1, Russell discloses, as claimed, a method in a computer system for executing code during a system management mode interrupt (Virtual System Mode Interrupt, see Col. 15, lines 60-61. Note the Wooten'299's Virtual System Mode is best reasonably and broadly interpreted as the claimed System Management Mode), the method comprising: upon occurrence of a system management mode interrupt (Virtual System Mode Interrupt, see Col. 15, lines 60-61), saving state (such as EIP, and EFLAGS, see Col. 15, lines 36-41, or Col. 16, lines 38-42) of the computer system; switching the computer system to protected mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E); executing 32-bit code (note the Wooten'299's protected mode is a flat 32 bit model) using the second global descriptor table (segment descriptor 402, see Fig. 4); and upon completion of the execution of the 32-bit code, restoring (see Col. 18, lines 27-37, regarding restoring the EIP register and the EFLAGS register) the saved state of the computer system; and returning (by IRET instruction, see Col. 18, lines 33-37) restoring from the occurrence of the interrupt.

Wooten'299 does not expressly disclose a global descriptor table register or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second

contents that point to a second global descriptor table that is distinct from the first global descriptor table.

Russell teaches disclose a global descriptor table register (MVM Context Register 128; see fig. 1) or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table (see col. 8, lines 55-60).

Note that when a mode is switched, the processor uses a different set of registers. This includes the global descriptor table. When a switch occurs, the MVM context register would point to a new table different from the current table. When the processor changes back to the first mode, the MVM context register would be returned to the previous state.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Wooten'299 by adding a global descriptor table register and replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table, as taught by Russell, in order to efficiently run two execution environments (see col. 2, lines 55-65).

20. Referring to claim 5, Wooten'299 discloses, as claimed, a method in a computer system for executing code during a system management mode interrupt (Virtual System

Mode Interrupt, see Col. 15, lines 60-61), the method comprising: upon occurrence of a system management mode interrupt (Virtual System Mode Interrupt, see Col. 15, lines 60-61), switching the computer system to another mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E); executing code (the code running in the Wooten'299's protected mode) that uses a global descriptor table (segment descriptor 402, see Fig. 4) that is different from the global descriptor table in use when the system management mode interrupt occurred (note the segment descriptor 402, see Fig. 4, will be different when referring to different segments at the different state of the Wooten'299's system before and after interrupt occurrence).

Wooten'299 does not expressly disclose a global descriptor table register or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table.

Russell teaches disclose a global descriptor table register (MVM Context Register 128; see fig. 1) or replacing first contents of the global descriptor table register that point to a first global table in use when the system management mod interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table (see col. 8, lines 55-60).

For combination and motivation, see above regarding claim 1.

21. As to claims 2 and 9, Wooten'299 also discloses: the 32-bit code is an operating system kernel for loading and running programs (since in the Wooten'299's system, the operating system kernel certainly comprises programs for an interrupt handling; and loading and running are the certain operations therein) during the occurrence of the system management mode interrupt.

As to claims 3 and 10, Wooten'299 also discloses: the programs are Windows Portable Executable programs (since Windows NT operating system is intended to be used in the Wooten'299's system).

22. As to claims 4, 11 Wooten'299 also discloses: the computer system is based on an Intel Pentium processor (as indicated in Col. 4, lines 29-30).

23. As to claim 6, Wooten'299 also discloses: the method of claim 5 including upon completion of the execution of the code, returning (by IRET instruction, see Col. 18, lines 33-37) from the occurrence of the system management mode interrupt.

24. As to claim 7, Wooten'299 also discloses: the method of claim 5 including: saving state (such as EIP, and EFLAGS, see Col. 15, lines 36-41, or Col. 16, lines 38-42) of the computer system; and upon completion of the execution of the 32-bit code, restoring (see Col. 18, lines 27-37, regarding restoring the EIP register and the EFLAGS register) the saved state of the computer system; and returning (by IRET instruction, see Col. 18, lines 33-37) restoring from the occurrence of the interrupt.

25. As to claim 8 Wooten'299 also discloses: the method of claim 5 wherein the executing executes 32-bit (note the Wooten'299's protected mode is a flat 32 bit model).

26. As to claim 12, Wooten'299 also discloses: the computer system is based on an Intel-compatible processor (as indicated in Col. 4, lines 29-30).

27. As to claim 13, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the programs are selected from the group consisting of a remote console program, a remote boot program, a remote diagnostics program, a remote restart program, and a debugging program (see Col. 19, lines 15-67 and Col. 29, regarding the instruction set formats such as VMOVS; VTOP EAX, memory; and PROBER suitable for the set forth programs).

28. As to claim 14, Wooten'299 also discloses: the method of claim 5 wherein the other mode is protected mode (see the Wooten'299's protected mode in Fig. 3B, when VSM bit is not set in EFLAGS, see Fig. 2C; or VSM enable bit is not set in VSM enable register 238 see Fig. 2E).

29. As to claim 15, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes transparently (see Col. 17, lines 39-45) to the foreground operating system.

30. As to claim 16, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes even if the foreground operating system has crashed or stopped (see Col. 15, lines 9-67, and Col. 16, regarding the interrupts/exceptions).

31. As to claim 17, as best understood, Wooten'299 also discloses: the method of claim 5 wherein the code executes when the foreground operating system crashes or stops (see Col. 15, lines 9-67, and Col. 16, regarding the interrupts/exceptions).

32. Claims 33 and 34 recite equivalent limitations as claims 54 and 55. These claims are rejected for the same reasons.

33. Claims 43 and 44 recite equivalent limitations as claims 54 and 55. These claims are rejected for the same reasons.

34. Claims 47-53 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of common knowledge in the art.

35. As to claim 47, Examiner asserts that it was common knowledge at the time of the invention to use signals received on a package pin of the processor for interrupts.

The advantage of using processor pins for interrupts is to input external interrupts to the processor since the pins are the only means of communication in a typical processor.

36. As to claim 48, any pin with the functionality recited in claim 47 could be considered a SMI# package pin. The terminology makes no difference.

37. As to claim 49, Examiner asserts that it was common knowledge at the time of the invention to use an APIC bus for receiving interrupts. The advantage of using an APIC bus for interrupts is to allow external interrupts be efficiently transferred to a processor.

38. As to claim 50, Examiner asserts that it was common knowledge at the time of the invention to use a front side bus for receiving interrupts. The advantage of using a front side bus for interrupts is to allow external interrupts be efficiently transferred to a processor.

39. As to claims 51-53, Examiner asserts that it was common knowledge at the time of the invention to send interrupts from the Northbridge and Southbridge controller (both are processor chips). The advantage of sending interrupts from Northbridge and Southbridge controllers is to allow external hardware to interrupt the processor.

40. As to claim 56, Examiner asserts that it was common knowledge at the time of the invention to upon completion of an interrupt, changing the contents of a hardware register indicating the cause of the interrupt. One advantage of indicating the cause of the interrupt is to add debug information for executing code.

41. Claims 26-32, 35-42 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wooten'299 in view of Russell and in further view of common knowledge in the art.

42. Claims 26-32 and 35 recite equivalent limitations as claims 47-53 and 56. The claims are rejected for the same reasons.

43. Claims 36-42 and 45 recite equivalent limitations as claims 47-53 and 56. The claims are rejected for the same reasons.

Response to Arguments

44. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

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45. Applicant's arguments with respect to claims 18-25 have been fully considered but they are not persuasive.

46. Applicant states:

Claim 18 recites a system management mode interrupt routine that, among other acts, switches the processor to protected mode. Applicant notes that a system management mode interrupt routine is executed in response to a system management mode interrupt. Wooten simply does not disclose switching the processor to protected mode as part of entering virtual system mode. As a first matter, Wooten indicates at 7:20- 23 that, "virtual system mode selection is controlled by a bit in the VSM Enable Register 238, discussed below, and is independent of the user mode and therefore does not affect the use of the PG, PE or VM bits," discussed elsewhere in Wooten as defining the user modes of operation of the processor, i.e., real, protected, or virtual 8086 mode. If this means of entering virtual system mode is independent of user mode, then entering virtual system mode has no effect on the user mode that is selected, and does not involve switching the processor to protected mode. At various other points such as 3:20-23, 3:35- 38, 10:34-37, and 10:43-45, Wooten makes clear that, rather than causing the processor to enter into any new user mode, entry into virtual system mode quite intentionally retains the user mode that was in use prior to entering VSM. That is, if the processor is in real mode when VSM is entered, it retains real mode; if the processor is in protected mode when VSM is entered, protected mode is retained; and if the processor is in virtual 8086 mode when VSM is entered, virtual 8086 mode is retained. Under no conditions does entry into VSM cause the processor to switch to protected mode from any other user mode upon entering VSM. To the extent that Wooten can be said to describe entering a different mode upon entering virtual system mode, this mode is virtual system mode itself, not a different user mode such as protected mode. Accordingly, claim 18 is patentable over Wooten, as are its dependent claims 19-25 and 46-56.

Examiner disagrees. Claim 18 merely recites the method comprises entering protected mode. Claim 18 does not recite any limitations which connect the switch to protected mode to any other limitations in the claim. As claimed, there method (method of using the processor) merely must switch to protected mode; there is no mention of connection to any other actions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 9:00 am - 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JM 10/2/06

Jesse R Moll
Examiner
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